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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/920,937	08/03/2001	Val Gont	0811.1220000	8800

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EXAMINER	
BHATNAGAR, ANAND P	

ART UNIT	PAPER NUMBER
2623	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,937	GONT ET AL.	
	Examiner	Art Unit	
	Anand Bhatnagar	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's amendment filed on 11/15/04 has been entered and made of record.

2. Applicant has amended claims 1, 14, and 15. Currently claims 1-17 are pending.

3. Applicant's arguments, see remarks pages 7-12, filed on 11/15/04, with respect to the rejection(s)of claim(s) 1-17 under 35Usc 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Meares (U.S. patent 6,230,305 B1) and Yamashita et al. (U.S. patent 5,568,397). Examiner refers to the rejection below.

DETAILED ACTION

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 14, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Meares (U.S. patent 6,230,305 B1).

Regarding claims 1-5 and 14: Meares discloses an editor in a computer system for a schematic having a number of pages (fig. 4, col. 1 lines 5-11, and col. 2 lines 18-24, wherein a schematic contains one or more layers. The layers are read as "pages.") comprising:

a module for cutting a selected portion of the schematic from any one of the schematic pages (col. 6 lines 20-25), each page displaying a viewable area of the schematic at a given time within the editor (col. 2 lines 35-40, wherein the layers, i.e. read as "pages," are displayed. The time of displaying the layer(s) is read as "at a given time" and this displaying is performed in the editor.);

a module for pasting the cut portion of the schematic onto any one of the schematic pages (col. 6 lines 22-25, wherein the editing is performed by cutting and pasting);

a module for connecting nets having the same label located on the same schematic page (col. 6 lines 10-25, wherein the editing is performed by cutting and pasting and the interconnections and symbols are kept intact throughout the layers).

Regarding claim 2: An editor as claimed which further includes a module for searching for objects within the schematic netlist (col. 6 lines 10-22 and 39-45, wherein a modification made in one layer is stored in the memory and the same modification is performed on other similar layers, i.e. the processor needs

to search which other layers are similar and contain the same elements in order to perform the same modification).

Regarding claim 3: An editor as claimed wherein the object is a signal label (col. 6 lines 39-45, wherein the interconnections are read as signal labels).

Regarding claim 4: An editor as claimed wherein the module provides a list of signal labels found on a pre-selected schematic page (col. 2 lines 20-32, wherein the symbols and interconnections are tracked on the different layers).

Regarding claim 5: An editor as claimed wherein the module provides a list of pages on which the signal label is found (col. 2 lines 20-32,wherein the symbols and interconnections are tracked on the different layers).

Regarding claim 15: A computer-readable medium as claimed wherein the project viewer software controls output schematic symbols and enables a user to view, trace and search objects throughout the project netlist data (col. 2 lines 50-55).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A.) Claims 6-9 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meares (U.S. patent 6,230,305 B1) in view of Yamashita et al. (U.S. patent 5,568,397).

Regarding claim 6: An editor as claimed wherein the object is a cell.

Meares discloses a schematic editing system wherein multiple layers/pages can be modified based on modification made on a single layer. Further, Meares discloses to i) create netlists, ii) track the elements, symbols, interconnections between layers, iii) obtain other associated information about the layers, iv) etc. (Meares; col. 2 lines 18-25). Meares does not disclose wherein the object is a cell. Yamashita et al. teaches to wherein an object are terminals (read as "cells" since only a terminal region of the schematic is analyzed) and editing is performed by using the terminal coordinates, terminal attribute information, and/or terminal name (Yamashita et al.; col. 4 lines 30-65). It would have been obvious to one skilled in the art to combine the teaching of Yamashita et al. to that of Meares because they are analogous in editing circuit schematics/diagrams. One in the art would have been motivated to incorporate the teaching of Yamashita et al. to that of Meares to decreasing the possibility of operator error while providing an efficient procedure for a designer to follow in the entering of signal names (Yamashita et al. col. 2 lines 58-61).

Regarding claim 7: An editor as claimed wherein the module provides a list of cells found on a pre-selected schematic page. See claims 4 and 6.

Regarding claim 8: An editor as claimed wherein the cell may be searched using one of the following: cell coordinates, name label or attributes. See claim 6.

Regarding claim 9: An editor as claimed wherein the module provides a list of schematic pages on which the cell is found. See claim 6.

Regarding claim 17: A process in a computer system as claimed wherein the hierarchal structure is organized by schematic pages (Yamashita et al.; col. 4 lines 49-53).

B.) Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meares (U.S. patent 6,230,305 B1).

Regarding claim 10: An editor as claimed in which further includes a module for eliminating extra pins or segment endings on a schematic. See claim 12.

Regarding claim 11: An editor as claimed which further includes a module for rendering invisible the labels on a current active page or on all of the schematic pages (Meares; col. 6 lines 15-20, wherein information can be added or deleted from the layers. The deletion of data is read as making labels and/or elements invisible).

Regarding claim 12: An editor as claimed which further includes a module for adding IN/OUT elements to pin segments.

Meares discloses to edit a schematic wherein information can be added or deleted from the layers. Meares does not teach to add IN/OUT elements to pin

segments. It would have been obvious tio one skilled in the art to modify the system wherein this would be part of the editing system since information already can be added or deleted from the schematics.

Regarding claim 13: An editor as claimed which further includes a module for cutting a net on a schematic and providing a signal label to the two cut ends of the net. See claim 12.

C.) Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meares (U.S. patent 6,230,305 B1), as modified by Yamashita et al. (U.S. patent 5,568,397), and further in view of Rostoker et al. (U.S. patent 5,544,067).

Regarding claim 16: A process in a computer system for interactively viewing netlist data from a high level schematic including schematic page numbers, cell names, nets, signal labels and segments, the viewing process comprising: It is rejected for the same reason as claim 8 above and for the following limitations of: generating the hierarchal structure of the schematic on one pane of a split screen and generating a selected part of the schematic on another pane of the split screen.

Meares discloses to display layers on a display along with the corresponding layer information such as symbols, interconnections, etc. on a display (col. 2 lines 20-30). Meares does not disclose to display structure on a pane of a split screen and on another pane display the schematics. Rostoker et al. teaches to display on a single display screen in different panes design and

results of a schematic (Rostoker et al.; figs. 14 and 15, col. 25 lines 61-67, and col. 26 lines 1-67). It would have been obvious to one skilled in the art to combine the teaching of Rostoker et al. to that of Meares, as modified by Yamashita et al., because they are analogous in schematic circuit designing. One in the art would have been motivated to incorporate the teaching of Rostoker et al. to the system of Meares, as modified by Yamashita et al., modified wherein information of interest to the user and/or schematics can be displayed in the panes in a single screen so that a user may display the output of several software programs at once on different portions of the display screen (Rostoker et al.; col. 5 lines 56-63).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anand Bhatnagar whose telephone number is (571) 272-7416, whose supervisor is Amelia Au whose number is (571) 272-7414, group fax is 703-872-9306, and Tech center 2600 customer service office number is 703-306-0377.

AB

Anand Bhatnagar

Art Unit 2623

May 27, 2005

SAMIR AHMED
PRIMARY EXAMINER